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10/790,058	03/02/2004	Yoshinori Wakimoto	118755	9834

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,058	WAKIMOTO ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,6,8,10 and 12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4,6,8,10 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/28/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed August 28, 2006 in response to the Office action dated March 27, 2006. Claims 2-4, 6, 8, 10, and 12-14 have been amended. Claims 1, 5, 7, 9, and 11 have been canceled. Claims 2-4, 6, 8, 10, and 12-14 are pending in this application.

OBJECTIONS

Drawings

1. In view of Applicant's amendment, the objections to the drawings have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

2. In view of Applicant's amendment, the 112 rejections to **claims 1 and 13** have been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa et al. (Patent Abstracts of Japan, "Associative Memory," Publication No. 2001-236790, published August 31, 2001) in view of Kanazawa et al. (U.S. Patent Application Publication 2002/122337).

5. **As per claim 2**, Yoshizawa discloses a CAM device comprising:

a CAM array including a plurality of physical banks (paragraph 0011, lines 1-3; Fig. 1, element 12); *It should be noted that "associative memory array" is analogous to "CAM array."*

a logical bank-physical bank converter for setting the assignment between logical banks and physical banks, and for outputting a control signal to set the configuration of a physical bank assigned to the logical bank, depending on a logical bank signal indicating a logical bank to be searched (paragraph 0012, lines 1-4; paragraph 0022, lines 1-4; Fig. 1, element 14); *It should be noted that "logic and physical signal transformation circuit" is analogous to "logical bank-physical bank converter", "logic bank" is analogous to "logical bank", and "CONFIG <2:0>" is analogous to "control signal to set the configuration of a physical bank assigned to the logical bank."*

a priority circuit for outputting search results in accordance with predetermined priority (paragraph 0015, lines 1-4; Fig. 1, element 16). *It should be noted that "priority network" is analogous to "priority circuit", "HHA <14:0>" and "HEA <14:0>" are analogous to "search results."*

Yoshizawa does not expressly disclose in searching, if the CAM device includes no physical bank assigned to the logical bank to be searched, the logical bank-physical bank converter outputs a signal to inform that there is no physical bank assigned to the logical bank.

Kanazawa discloses in searching, if the CAM device includes no physical bank assigned to the logical bank to be searched, the logical bank-physical bank converter outputs a signal to inform that there is no physical bank assigned to the logical bank (paragraphs 0080-0081; Figs. 5 and 6). *It should be noted that whenever the signal "$OROUT_{i+1}$" is output the signal indicates that there is a defective CAM word (i.e. there is no physical word assigned to a logical word).*

Yoshizawa and Kanazawa are analogous art because they are from the same field of endeavor, that being cascaded content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Kanazawa's shift circuitry with Yoshizawa's CAM array, logic and physical signal transformation circuit, and priority circuit.

The motivation for doing so would have been to provide a spare CAM word as a redundant circuit without increasing a circuit scale and an output delay time, but rather improve product yield (Kanazawa, paragraph 0023, lines 4-6).

Therefore, it would have been obvious to combine Yoshizawa and Kanazawa for the benefit of obtaining the invention as specified in claim 2.

6. **As per claim 4**, the combination of Yoshizawa/Kanazawa discloses when searching is performed, the logical bank-physical bank converter outputs, to each

physical bank assigned to the logical bank to be searched, a control signal for dynamically setting the configuration of the physical bank (Yoshizawa, paragraph 0030, lines 1-3; Fig. 1). *It should be noted that "SRCH" is analogous to the "control signal for dynamically setting the configuration of the physical bank."*

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa view of Kanazawa as applied to claim 2, and in further view of Pereira et al. (U.S. Patent 6,493,793).

8. The combination of Yoshizawa/Kanazawa discloses the logical bank-physical bank converter outputs the signal to the cascade circuit and, in response, to the signal, the cascade circuit outputs a signal indicating the CAM device includes no hit entry (Kanazawa, paragraphs 0051-0052; Fig. 1). *It should be noted that the "HHA [7:0]" is analogous to the "signal indicating the CAM device includes no hit entry."*

The combination of Yoshizawa/Kanazawa does not expressly disclose a cascade circuit for performing a logical operation on the search results output from the priority circuit of the CAM device and search results supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device.

Pereira discloses a cascade circuit for performing a logical operation on the search results output from the priority circuit of the CAM device and search results supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device (col. 4, lines 48-51; col. 4, line 63 – col. 5, line 1; col. 5, lines 59-60; col. 6, lines 18-25; Fig. 1, element 100; Fig. 2, elements 204 and 205). *It should be noted that "cascade logic circuit" is analogous to "cascade circuit",*

"match flag logic" is analogous to "priority circuit", "/MFO" is analogous to "search results", "high-priority" is analogous to "high-order" and "low-priority" is analogous to "low-order."

The combination of Yoshizawa/Kanazawa and Pereira are analogous art because they are from the same field of endeavor, that being cascaded content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Pereira's cascade logic circuit with Yoshizawa/Kanazawa's CAM array, logic and physical signal transformation circuit, priority circuit, and shift circuitry.

The motivation for doing so would have been to gain the benefit of cascading a number of memory devices in a manner that achieves a balance between the number of match flag input pins and the time required to generate the system match flag (Pereira, col. 2, lines 43-45).

Therefore, it would have been obvious to combine Yoshizawa/Kanazawa and Pereira for the benefit of obtaining the invention as specified in claim 3.

9. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa in view of Kanazawa as applied to claims 2 and 4 above, and in further view of Lyon (U.S. Patent 6,493,812).

The combination of Yoshizawa/Kanazawa discloses all the limitations of claims 6 and 8 except the logical bank-physical bank converter is capable of assigning one physical bank to two or more different logical banks.

Lyon discloses the logical bank-physical bank converter is capable of assigning one physical bank to two or more different logical banks (col. 2, lines 7-11). *It should be noted that "virtual" is analogous to "logical." It should also be noted that setting an assignment between virtual banks to physical banks the real procedure that is taking place is an assignment setting between the virtual and physical addresses of the banks.*

The combination of Yoshizawa/Kanazawa and Lyon are analogous art because they are from the same field of endeavor, that being addressing memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Lyon's virtual address aliasing technique within Yoshizawa/Kanazawa's logic and physical signal transformation circuit.

The motivation for doing so would have been to increase memory performance by allowing cache data to be retained for multiple users and also access the cache data through different virtual addresses as the users change (Lyon, col. 7, lines 62-65).

Therefore, it would have been obvious to combine Yoshizawa/Kanazawa and Lyon for the benefit of obtaining the invention as specified in claims 6 and 8.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa in view of Kanzawa as applied to claim 2 above, and in further view of Pereira as applied to claim 3 above, and in even further of Khanna et al. (U.S. Patent 6,393,514).

The combination of Yoshizawa/Kanazawa/Pereira discloses all of the limitations of claim 10 except said cascade circuit outputs signal HO as logical OR on a signal HIT of

the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI.

Khanna discloses said cascade circuit outputs signal HO as logical OR on a signal HIT of the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI (col. 5, lines 35-43; col. 6, lines 41-45; Fig. 6, element 32; Fig. 7, element 64). *It should be noted that "match" is analogous to "hit." It should also be noted that the incorporated reference, Khanna (U.S. Patent 6,175,513), discloses an OR gate that inputs various multiple match flags and outputs an overall multiple match flag.*

The combination of Yoshizawa/Kanazawa/Pereira and Khanna are analogous art because they are from the same field of endeavor, that being content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Khanna's multiple match flag logic and full flag logic within Yoshizawa/Kanazawa/Pereira's cascade logic circuit.

The motivation for doing so would have been to decrease the time delay between write instructions which causes valid data to be written to the last available CAM row and assertion of the full flag (Khanna, col. 1, line 66 – col. 2, line 2).

Therefore, it would have been obvious to combine Yoshizawa/Kanazawa/Pereira and Khanna for the benefit of obtaining the invention as specified in claim 10.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa in view of Kanzawa as applied to claim 2 above, and in further view of Lyon as applied to claim 4 above, and in even further of Pereira and Khanna.

12. The combination of Yoshizawa/Kanazawa/Lyon discloses all the limitations of claim 12 except a cascade circuit for performing a logical operation on the search results output from the priority circuit of the CAM device and a search results supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device,

wherein said cascade circuit outputs signal HO as logical OR on a signal HIT of the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI.

Pereira discloses a cascade circuit for performing a logical operation on the search results output from the priority circuit of the CAM device and a search results supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device (col. 4, lines 48-51; col. 4, line 63 – col. 5, line 1; col. 5, lines 59-60; col. 6, lines 18-25; Fig. 1, element 100; Fig. 2, elements 204 and 205). *See the citation note for claim 3 above.*

The combination of Yoshizawa/Kanazawa/Lyon and Pereira are analogous art because they are from the same field of endeavor, that being cascaded content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Pereira's cascade logic circuit with

Yoshizawa/Kanazawa/Lyon's CAM array, logic and physical signal transformation circuit, priority circuit, and shift circuitry.

The motivation for doing so would have been to gain the benefit of cascading a number of memory devices in a manner that achieves a balance between the number of match flag input pins and the time required to generate the system match flag (Pereira, col. 2, lines 43-45).

The combination of Yoshizawa/Kanazawa/Lyon/Pereira does not expressly disclose said cascade circuit outputs signal HO as logical OR on a signal HIT of the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI.

Khanna discloses said cascade circuit outputs signal HO as logical OR on a signal HIT of the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI (col. 5, lines 35-43; col. 6, lines 41-45; Fig. 6, element 32; Fig. 7, element 64). *See the citation note for claim 10 above.*

The combination of Yoshizawa/Kanazawa/Lyon/Pereira and Khanna are analogous art because they are from the same field of endeavor, that being content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Khanna's multiple match flag logic and full flag logic within Yoshizawa/Kanazawa/Lyon/Pereira's cascade logic circuit.

The motivation for doing so would have been to decrease the time delay between write instructions which causes valid data to be written to the last available CAM row and assertion of the full flag (Khanna, col. 1, line 66 – col. 2, line 2).

Therefore, it would have been obvious to combine Yoshizawa/Kanazawa/Lyon, Pereira, and Khanna for the benefit of obtaining the invention as specified in claim 12.

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa view of Kanazawa and Pereira.

14. Yoshizawa discloses a CAM device comprising:

a CAM array including a plurality of physical banks (paragraph 0011, lines 1-3; Fig. 1, element 12); *See the citation note for the similar limitation in claim 2 above.*

a logical bank-physical bank converter for setting an assignment between logical banks and physical banks, and for outputting a control signal to set a configuration of a physical bank assigned to a logical bank to be searched, depending on a logical bank signal indicating the logical bank to be searched, to the physical bank assigned to the logical bank to be searched (paragraph 0012, lines 1-4; paragraph 0022, lines 1-4; Fig. 1, element 14), *See the citation note for the similar limitation in claim 2 above.*

a priority circuit for outputting search results in accordance with predetermined priority (paragraph 0015, lines 1-4; Fig. 1, element 16). *See the citation note for the similar limitation in claim 2 above.*

Yoshizawa does not expressly disclose while when the CAM device includes no physical bank assigned to the logical bank to be searched, a signal is output to indicate that there is no physical bank assigned to the logical bank;

and a cascade circuit for performing a logical operation on the search results output from the priority circuit of the present CAM device and a search results supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device.

Kanazawa discloses while when the CAM device includes no physical bank assigned to the logical bank to be searched, a signal is output to indicate that there is no physical bank assigned to the logical bank (paragraphs 0080-0081; Figs. 5 and 6). *See the citation note for the similar limitation in claim 2 above.*

Yoshizawa and Kanazawa are analogous art because they are from the same field of endeavor, that being cascaded content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Kanazawa's shift circuitry with Yoshizawa's CAM array, logic and physical signal transformation circuit, and priority circuit.

The motivation for doing so would have been to provide a spare CAM word as a redundant circuit without increasing a circuit scale and an output delay time, but rather improve product yield (Kanazawa, paragraph 0023, lines 4-6).

The combination of Yoshizawa/Kanazawa does not expressly disclose a cascade circuit for performing a logical operation on the search results output from the priority circuit of the CAM device and search results supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device.

Pereira discloses a cascade circuit for performing a logical operation on the search results output from the priority circuit of the CAM device and search results

supplied from a higher-order CAM device, and transmitting the results of the logical operation to a lower-order CAM device (col. 4, lines 48-51; col. 4, line 63 – col. 5, line 1; col. 5, lines 59-60; col. 6, lines 18-25; Fig. 1, element 100; Fig. 2, elements 204 and 205). *See the citation note for the similar limitation in claim 3 above.*

The combination of Yoshizawa/Kanazawa and Pereira are analogous art because they are from the same field of endeavor, that being cascaded content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Pereira's cascade logic circuit with Yoshizawa/Kanazawa's CAM array, logic and physical signal transformation circuit, priority circuit, and shift circuitry.

The motivation for doing so would have been to gain the benefit of cascading a number of memory devices in a manner that achieves a balance between the number of match flag input pins and the time required to generate the system match flag (Pereira, col. 2, lines 43-45).

Therefore, it would have been obvious to combine Yoshizawa, Kanazawa, and Pereira for the benefit of obtaining the invention as specified in claim 13.

15. Claim 14 is rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa in view of Kanzawa and Pereira as applied to claim 13 above, and in further of Khanna.

16. The combination of Yoshizawa/Kanazawa/Pereira discloses all of the limitations of claim 10 except said cascade circuit outputs signal HO as logical OR on a signal HIT

of the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI.

Khanna discloses said cascade circuit outputs signal HO as logical OR on a signal HIT of the CAM device and an input signal HI, and outputs signal FLO as logical AND on a signal FULL and an input signal FLI (col. 5, lines 35-43; col. 6, lines 41-45; Fig. 6, element 32; Fig. 7, element 64). *See the citation note for claim 10 above.*

The combination of Yoshizawa/Kanazawa/Pereira and Khanna are analogous art because they are from the same field of endeavor, that being content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Khanna's multiple match flag logic and full flag logic within Yoshizawa/Kanazawa/Pereira's cascade logic circuit.

The motivation for doing so would have been to decrease the time delay between write instructions which causes valid data to be written to the last available CAM row and assertion of the full flag (Khanna, col. 1, line 66 – col. 2, line 2).

Therefore, it would have been obvious to combine Yoshizawa/Kanazawa/Pereira and Khanna for the benefit of obtaining the invention as specified in claim 10.

Response to Arguments

17. The indicated allowability of **claims 2, 4, 6, 8, 10, and 12-14** is withdrawn in view of the newly discovered reference to Kanazawa et al. (U.S. Patent Application

Publication 2002/122337). Rejections based on the newly cited reference are presented above.

18. Applicant's arguments with respect to **claims 2-4, 6, 8, 10, and 12-14** have been considered but are moot in view of the new grounds of rejection as presented above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 2-4, 6, 8, 10, and 12-14** have received a second action on the merits and are subject of a second action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 6,480,931 (Buti et al.) discloses a non-conventional CAM and register mapper organization and circuit implementation is provided which allows simultaneous execution of a large number of CAM searches.

2. U.S. Patent 6,611,445 (Kanazawa et al.) discloses a content addressable memory (CAM), a spare CAM word serving as a redundant circuit is mounted in addition to a plurality of CAM words, and a storage section for holding information indicating whether there is a defective CAM word in the plurality of CAM words, and if there is one or more defective CAM word, address information of the defective CAM word.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
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November 6, 2006

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